

ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device,
including: a group of memory cells formed in X and Y
directions in and on a semiconductor substrate, the X and Y
5 directions crossing each other, each memory cell including
source and drain regions formed in the substrate, a first
insulating film formed on a surface of the substrate between
the source and drain regions, a floating gate formed on the
first insulating film, and a control gate formed above the
10 floating gate via a second insulating film; a plurality of
wordlines each connected to the control gates of the memory
cells in the X direction; a plurality of sub-bit lines, each
sub-bit line connected to a predetermined number of source
and drain regions of the memory cells in the Y direction; a
15 plurality of main-bit lines extending in the Y direction, each
main-bit line being connected to the sub-bit line in the Y
direction, and a plurality of dielectric layers laminated on the
sub-bit lines, wherein each main-bit line is formed on any one
of the plurality of dielectric layers, each main-bit line being
20 connected to the corresponding sub-bit line via a conductive
member penetrating through the dielectric layer under the
main-bit line, and adjacent two of the main-bit lines are
located on different dielectric layers.